LOW DISTORTION AND HIGH EFFICIENCY 17 W POWER GaAs FETS FOR SATELLITE COMMUNICATION SYSTEM APPLICATIONS

Hiroaki Tsutsui, Isao Takenaka, Hidemasa Takahashi, Kazunori Asano,
Junko Morikawa, Kohji Ishikura and Masaaki Kuzuhara
ULSI Device Development Laboratories, NEC Corporation
9-1, Seiran 2-Chome, Otsu, Shiga 520-0833, Japan

ABSTRACT

We have developed a GaAs FET power amplifier that demonstrated a high power-added efficiency of 68% with 17.1W output power and a 16dB linear gain at 1.5GHz. The developed 17W amplifier also exhibited state of the art low distortion characteristics of less than –21dBc NPR (Noise Power Ratio) at the 5dB-output power back-off point from 2dB-gain compression point. These excellent results are performed by optimizing the drain bias circuit as well as the internal matching network.

INTRODUCTION

There is an increasing requirement for an L-band power amplifier that satisfies extremely low distortion and high efficiency characteristics, both of which are of particular importance for the recent mobile communication satellites that employ common amplification for multi-carrier transmission.

In this work, we have newly designed the input and output matching circuits to maximize the power-added efficiency by a large signal simulation. In addition, the relationship between the distortion characteristics and the bias circuit impedance was experimentally clarified.

The developed 17W power GaAsFET amplifier featured both the high efficiency (68%) and the low distortion (-21dBc NPR) characteristics suitable for the satellite communication system applications.

DEVICE AND MATCHING NETWORK

We employed power GaAs MESFETs with 1.0 •m WSi gate fabricated in a step-recessed structure[1][2]. These devices exhibited typical Idss, Imax, transconductance, pinch-off voltage and drain breakdown voltage of 200 mA/mm, 340 mA/mm, 125 mS/mm, •-2.0 V and 25 V, respectively. The amplifier was designed to combine the output power of two FET chips with a total gate width of 70 (35×2) mm. The FET chips were assembled with impedance transforming circuits in a conventional ceramic package as shown in Fig. 1. The overall dimension of the amplifier is 24 mm×17.4 mm.
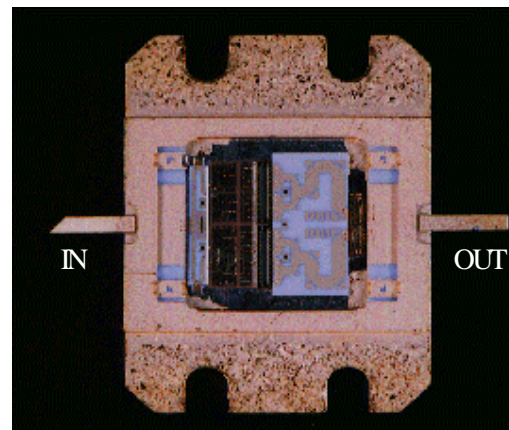

Figure1: top view of the internal matched device.

Fig. 2 shows the equivalent circuit of the internal matching network. The internal input matching network consists of a three-

input　　　matching　　FETs　output　　　matching

$ZS(f0)=1.0+j0.57\bullet$
$ZS(2f0)=0.29+j0.91\bullet$

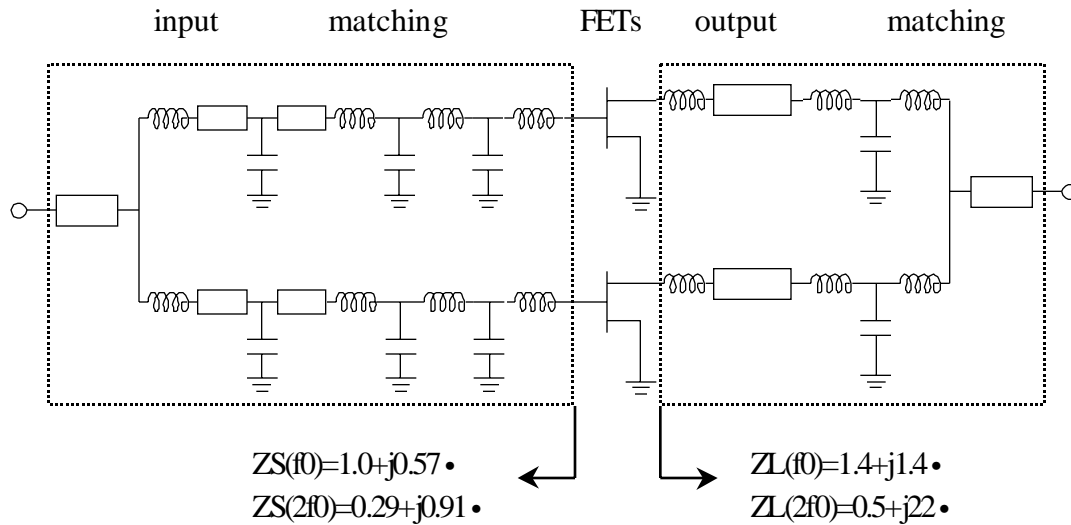$ZL(f0)=1.4+j1.4\bullet$
$ZL(2f0)=0.5+j22\bullet$

Figure2: An equivalent circuit of the developed amplifier.

stage LC low pass filter network, while the internal output matching circuit consists of a $\bullet$/8 transmission line for the fundamental frequency and an LC low pass filter network. These input and output matching circuits were optimized not only at the fundamental frequency (=1.5GHz) but also at the second harmonic frequency (=3GHz) to maximize power-added efficiency by employing a large-signal FET model simulation.

DISTORTION CHARACTERISTICS AND DRAIN BIAS CIRCUIT

It was reported that, when the output bias circuit impedance was high at the intermediate frequency of the 2-tones carriers, the RF carrier outputs were distorted by the amplitude modulation at the intermediate frequency [3]. In the case of multi-tone carrier, low frequency spurious signals are generated by the even-order distortion of an FET. Such spurious signals modulate the drain bias voltage in the same manner as the 2-tones case. The modulated drain bias voltage is mixed with the input signals, resulting in additional odd-order intermodulation distortion.

We have investigated the relationship between the distortion characteristics and the output bias circuit by measuring not only the IM3 (3rd-order intermodulation) but also NPR at various differential frequencies ($|f2-f1|$) for IM3 and various noise-band widths for NPR. Fig. 3 shows the output bias circuit used in our experiment. We varied the impedance of the output circuit by connecting a unit circuit consisting of 1/4$\bullet$line and capacitor in parallel (LC1$\bullet$LC4) or using another circuit consisting of 3/4$\bullet$line and capacitor (L3).
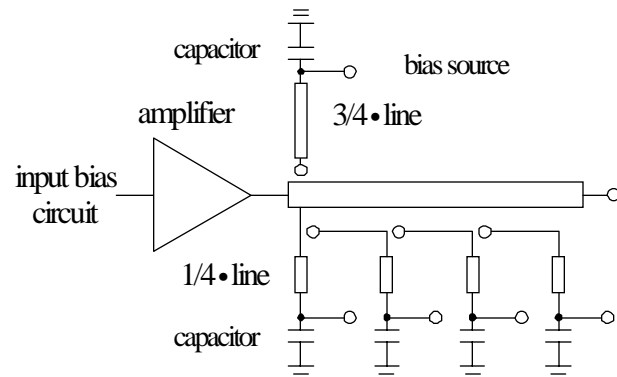

Figure3: Schematic of the output bias circuit used for the experiment.

Figure 4 shows the measured IM3, NPR as a function of the bias circuit impedance which is defined as the impedance calculated at the differential frequency for IM3 and at half of the noise-band width for NPR. It was found that IM3 and NPR are drastically degraded when the absolute value of the bias circuit impedance is higher than 1•. These results indicate that choosing low impedance value less than 1• in the low frequency range while ensuring sufficiently high impedance at the fundamental frequency is of great importance to suppress degradation in the distortion characteristics.

2dB Comp.•8V,0.5A

Figure 5: Noise output power and noise power added efficiency as a function of the output bias circuits impedance at half of the noise-band width frequency.
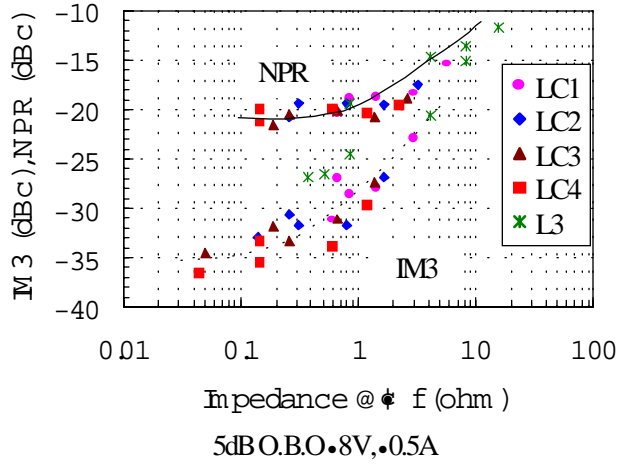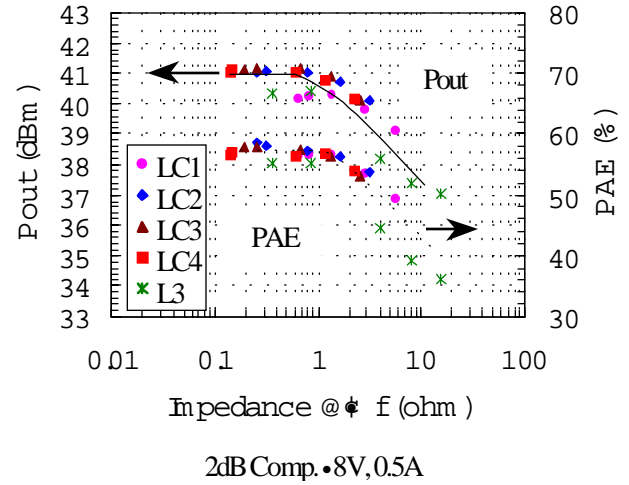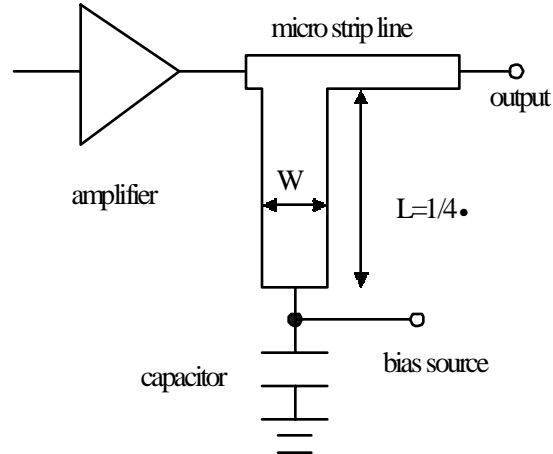
5dB O.B.O•8V,•0.5A

Fig. 4: NPR and IM3 at 5dB output power back-off point as a function of the output bias circuits impedance at the differential frequency for IM3 and at half of the noise-band width for NPR.

Fig. 5 shows the noise output power and noise power-added efficiency as a function of the output bias impedance at half of the noise-band width frequency. This figure indicates that the bias circuit impedance influences these characteristics. These degradations seem to be caused by the drain bias voltage swing at low frequency range.

Considering these results, we designed the output bias circuit as shown in Fig. 6. The impedance at half of the noise-band width of 10MHz is 0.53•. The impedance was

Figure 6: Schematic of the designed output bias circuit for L-band amplifier.

optimized by choosing the micro strip line width W.

AMPLIFIER PERFORMANCE

Measured output power and power-added efficiency versus input power are shown in Fig. 7. The fabricated FET demonstrated a high power-added efficiency of 68% with

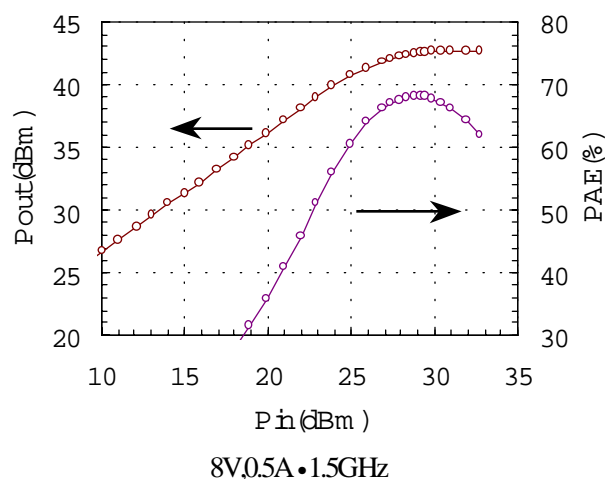17.1W output power with a 16dB linear gain (at 1.5GHz Vds=8V, Idq=3% of Idss).

8V,0.5A • 1.5GHz

Figure 7: Output power and power-added efficiency versus input power at 1.5GHz of the developed amplifier.
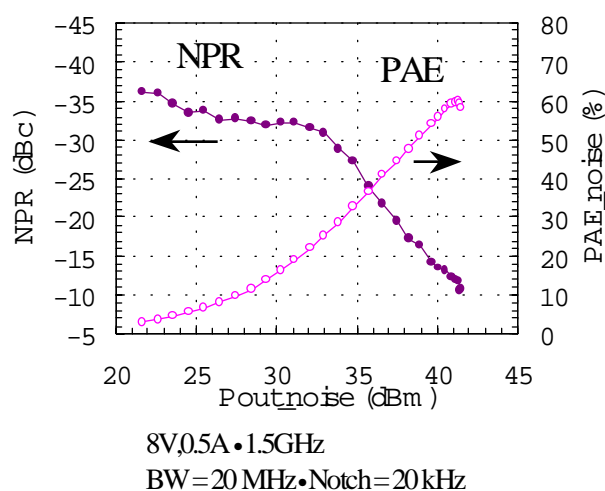

8V,0.5A • 1.5GHz
BW = 20 MHz • Notch = 20 kHz

Figure 8: Noise power ratio and noise power-added efficiency versus noise output power at 1.5GHz of the developed amplifier.

Fig. 8 shows the relationship between NPR, power-added efficiency and the output power. From Figs 7, 8, the low distortion performance of less than –21dBc NPR at the 5dB-output power back-off point from the 2dB-gain compression point is exhibited. At this compression point, noise power-added

efficiency still remains higher than 40%.

Consequently we could obtain the low distortion and high efficiency power amplifier which indicates not only good single-tone characteristics but also supreme multi-tone characteristics for practical use.

CONCLUSIONS

We have developed a GaAs FET power amplifier that demonstrated a high power-added efficiency of 68% with 17.1W output power and a 16dB linear gain at 1.5GHz. The developed 17W amplifier also exhibited state of the art low distortion characteristics of less than –21dBc NPR at the 5dB-output power back-off point from 2dB-gain compression point. The extremely high power-added efficiency and the excellent NPR characteristics of the developed device are very suitable for satellite communication system applications.

ACKNOWLEDGEMENTS

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